REMARKS

Favorable reconsideration and allowance of the claims of the present application, as amended, is respectfully requested.

In the present Office Action, the Examiner rejected Claims 1, 3-10 and 14-16 under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent No. 6,795,942 to Schwarz ("Schwarz ").

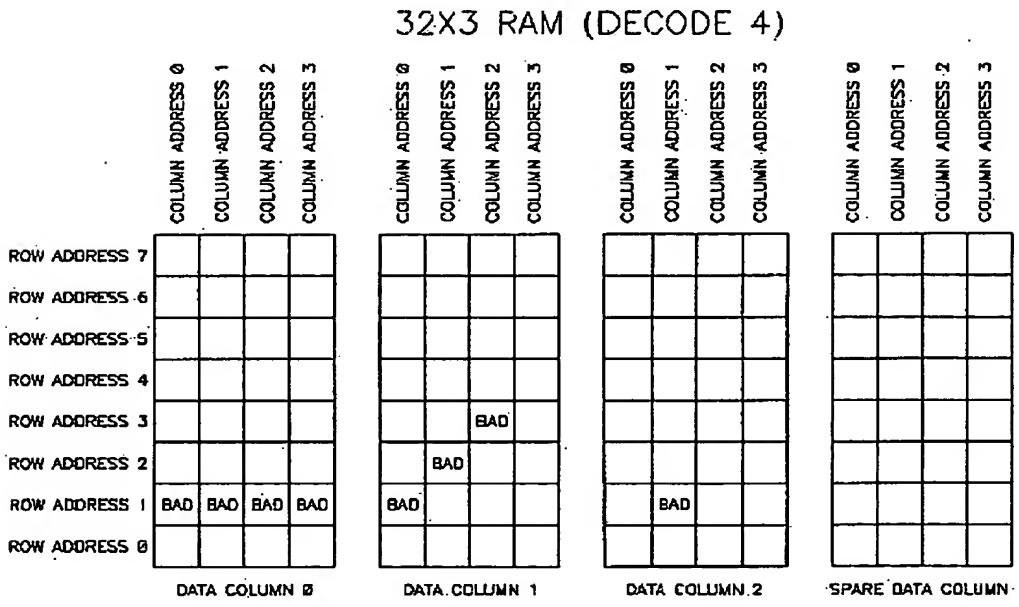
The Examiner did object to Claims 2 and 11-13, however did indicate that these claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In response, applicants cancel Claim 1 and incorporate the subject matter there in Claim 3 which is now cast in independent form. Respectfully, contrary to the Examiner's determination, new amended independent Claim 3 is allowable over the prior art to Schwarz.

With respect to specific differences between the present invention and Schwarz, it is important to note that, generally, Schwarz counts individual "defects" while the method of the present invention counts unique failing rows that have at least one defect. In other words if a particular unique row has several defects within the same data column, they can all be fixed by the same redundant row. Thus, in the method of the present invention, it is not necessary to care about the exact number of defects on that row.

Applicants note the use of the term data column which Claim 3 has been further amended to set forth, and which remaining dependent Claims 4-5, 7-8, 10-15 have been amended to set forth. The present invention, as described in the background section and description of the originally filed specification and in reference to Figure 1,

tests data columns as opposed to columns, per se, as in Schwarz (and are thus differentiated over Schwarz). To aid in the Examiner's understanding applicants provide the following Figure illustrating what is meant by a data column (also referred to as a databit) according to the invention as recited in the claims and herein the remarks:



This Figure illustrates a 32x3 RAM with a decode of four (4). The present invention provides that each data column will be tested one at a time (with the others being masked out) and the one with the highest number of unique failing row addresses will be replaced with a spare data column. Data column 0 has four bad memory cells but they are all on the same row address and thus from this invention's perspective there is only one fail. Data column 1 has three bad memory cells, but they

are all on unique rows and thus it will have a fail count of three. Data column 2 has only one bad memory cell and a fail count of 1. Therefore, in this example, Data column 1 would be replaced with a spare data column because it has the highest number of unique failing rows (it is the worst failing column), even though it doesn't have the highest number of failing cells.

It is respectfully submitted that no new matter is being entered in amended Claims 3-5, 7-8 and 10-15 by the clarifying recitation of the term data column as original support is found in the specification, Figures and claims, as filed.

Thus, with respect to the present invention, amended Claim 3 is patentably distinct from the teaching of Schwarz because Schwarz is about providing column redundancy (by performing true column testing within one databit (or data column), and thus can test one column at a time. Thus, in Schwarz, after a column is replaced, the original column is ignored in all further testing. In the present invention, as now claimed in amended Claim 3, both column and row redundancy, i.e., a "bit redundancy " scheme, is provided whereby all data within a data column (a databit), is being examined. The normal test logic has a global "pass/fail" signal for the cell under test of all databits, one data column (databit) at a time. In the present invention, one databit's data at a time is being examined, the data from all other databits is being "masked out" so that the global "pass/fail" signal can be used and then only relates to the databit under test. Clearly this is a different type of "masking" than Schwarz uses.

Respectfully, Claim 3, as amended, now sets forth allowable subject matter and the Examiner is respectfully requested to withdraw the rejection of Claim 3 under 35 U.S.C. §102(e). In light of the cancellation of Claim 1, dependent Claims 2, 10-11 and 14-16 are being further amended to properly depend upon the now

independent base Claim 3.

However, with respect to the other dependent Claims, applicants respectfully submit the following:

Claim 4 is allowable as setting forth the decoder scheme used in providing the masking of data columns that allows all databits except the one under test to be ignored. Schwarz is masking differently. Therefore, the decoder Claim 4 is allowable.

With respect to the rejection of Claim 5, the algorithm set forth in Claim 5 is neither taught nor suggested by Schwarz. Specifically, Col. 5, lines 4-20 of Schwarz describes testing a single column and replacing all that meet a certain threshold of errors. It mentions that those(plural) with the greatest number of defects would be replaced in this method and then ignored in further testing. Claim 5, on the other hand, is directed to two modes of memory usage whereby the memory has one particular input which is used differently depending on mode - during a BIST mode, the input is used to define the datbit to be tested; and, during a customer mode, the input is used to define the replaced databit (the worst one - precisely one, not plural). Respectfully, there is absolutely no equivalent teaching or suggestion in Schwarz and is certainly novel and unobvious in view of Schwarz.

With respect to the rejection of Claim 6, it is submitted that this claim is directed to the counting of unique failing rows that contain defects and not the defects in and of themselves- a concept that is neither taught nor suggested by Schwarz.

With respect to the rejection of Claim 7, it is submitted that this claim is directed to the method of finding the "worst" (singular) data column (i.e., databit). Once a databit has an error, it is defined as the worst. Anytime another databit has a higher

number of unique row fails, then that column becomes the worst and the error count and databit number are stored. Schwarz, on the other hand, compares each column's fail count against a stored value and if it is higher than that, then the column is flagged for repair and its address is stored. Several columns can meet this threshold. That is how the "worst" (plural) in Schwarz get fixed. The "underflowing" referred to in Schwarz, e.g., col. 6, lines 30-51 takes into account the total number of extra columns - if too many columns meet the threshold, then their memory is unrepairable.

With respect to the rejection of Claim 8 directed to implementing the spare column prior to the second pass of the self-test, Schwarz does all its testing on the "real", "non-extra" columns during all testing. When Schwarz hits a flagged column it just ignores its output. Claim 8, on the other hand, states that between the first and second pass of test, the calculated solution is implemented. This means that during pass two the worst column is already replaced and so an error in the replaced column is now a "real fail" (in the extra column that has been steered to the failing column).

With respect to the rejection of Claim 9 directed to implementing the FAR register that stores unique failing row addresses such that, at the end of the second pass of self-test, the FAR values are used to allocate and implement the spare rows, Applicants are hard-pressed to find any teaching or suggestion of this in Schwarz. Claim 9 particularly is directed to re-using the same register that stores the unique failing row information (per databit) during the second pass of test. In other words, only one set of registers are used in both passes of test. To the contrary, Figure 3 of Schwarz shows use of two registers referenced as elements 106 and 122. Reading at Column 10, lines 4-29 of Schwarz confirms this - they are not sharing registers but instead have "analagous" circuitry.

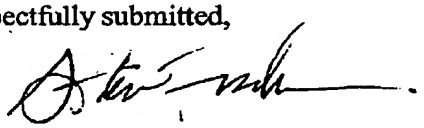
With respect to the rejection of Claim 10 directed to implementing the BIST and the decoder for data column selection, in sum the invention implements one set of circuitry that is used differently depending on which pass of testing is being implemented, BIST or customer mode.

With respect to the rejection of Claim 14 directed to dividing RAM into sections of adjacent columns, with each section having its own redundant column to replace a worst failing column in that section, and each section is tested in parallel with other sections of columns, applicants reiterate the aforementioned distinction that the present invention replaces databits as compared to Schwarz that replaces columns within a databit. Through Schwarz column 10, Schwarz refers to a memory with a single databit. However, at col. 11, lines 22-50 and in reference to Schwarz Figure 4, Schwarz attempts to expand its application to include multiple databits; however, in Schwarz, each databit works like the singular one described earlier. On the other hand, the present invention includes one redundant databit that is adapted to "service" many databits. The present invention as set forth in Claim 14 states that at some point when a second extra databit is needed, the space is partitioned up so that each spare databit can only replace a bad databit within its region (Claim 14). In Schwarz however, any spare column can replace any bad column within the databit. Furthermore, in the present invention, each of the regions are tested in parallel -so testing is done in half the time. In other words, in an example implementation from which Claim 14 reads, if memory of 80 databits is provided with two spare databits, spare databit 1 can replace any bad databit from 1-40 and spare databit 2 can relace any bad databit from databits 41-80. According to the invention, databits 1 and 41 are tested in parallel for rows with defects, 2 and 42 are tested in parallel, and so on. What Schwarz describes as a "bank" is

analogous to what is referred to herein as a "databit", and from the reading of Schwarz, he would test databits 1-80 in serial and then be able to replace any bad two with the spare two. Schwarz method would thus be slower than the method of the present invention and inherently different.

In view of the foregoing amendments and remarks, this application is now believed to be in condition for allowance, and a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,



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